## ABSTRACT OF THE DISCLOSURE

A phase-lock loop which includes an oscillator having an oscillator signal whose frequency is related to a received error correction signal and phase-frequency detector receiving and comparing the oscillator signal and a reference signal from the master circuit and generating the error correction signal based on the phase difference of the oscillator signal and the reference signal. A first window circuit counts the number of comparing cycles of the detector and provides a first window signal for the transmission of the error correction signals from the detector to the oscillator at a frequency of a predetermined number of counted comparing cycles. A second window circuit which, in response to at least the oscillator signal, narrows the first window signal to limit the duration of the correction signal for irregular reference signals.